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Examiner Phuongchau Ba Nguyen	USPTO GAU - 2665 Confirmation No.: 1241	1-571-273-3148	

Date	Client/Matter Number
March 20, 2006	100794-00171 (FUJS 14.330A)
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**** EXPEDITED PROCEDURE ****

Serial No.: 09/989,858

3 pages – INTERVIEW AGENDA

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Serial No. 09/989,858
Page 1 of 3**Attorney Docket No.: FUJS 14.330A (100794-00171)****IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Inventor(s) : Yoshinori NAKAMURA et al.

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Serial No. : 09/989,858

Filed : November 16, 2001

Title : **FRAME SYNCHRONOUS PATTERN PROCESSING APPARATUS AND FRAME SYNCHRONOUS PATTERN DETECTION APPARATUS AND METHOD FOR DETECTING FRAME SYNCHRONOUS PATTERN**

Examiner : Phuongchau Ba Nguyen

Group Art Unit : 2665

Confirmation No. : 1241

March 20, 2006

INTERVIEW AGENDA

Applicants and their undersigned representative, Mr. Dexter Chang (Reg. No. 44,071), thank the Examiner for his time and consideration for a telephone interview to be conducted on Tuesday, March 21, 2006 at 10:00 am between the Examiner and Mr. Chang. Applicants respectfully submit the following as a brief outline of the agenda for the interview.

1. Double Patenting Rejection

Applicants respectfully submit that U.S. Patent No. 6,385,213 issued from Application No. 08/880,723 filed on June 23, 1997, which is the parent to the present application. As such,

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U.S. Patent No. 6,385,213 carries the same term as any patent that may issue from the present application. And the present application, therefore, cannot extend the "right to exclude" of U.S. Patent No. 6,385,213. Applicants, thus, respectfully submit that a terminal disclaimer is unnecessary in that the present application would have no extended term to disclaim.

2. 35 U.S.C. § 102 Rejection

Applicants would like to point out that U.S. Patent No. 5,710,774 to Suh et al., as cited and relied upon by the Examiner, does not disclose

"said provisional-region detection section being for sampling, from parallel data according to a synchronous digital hierarchy (SDH) transmission system, a part of the parallel data in which said actual frame synchronous pattern is presumably included, as provisional region data and for outputting the provisional region data in serial form to said frame synchronous pattern detecting section," of the claimed invention. (Emphasis added)

In particular, Applicants would like to point out that comparison signals X1 and X2, which are selected by selecting circuit 60, described in Suh et al. are comparison signals of the parallel data output from serial/parallel converter 10. Therefore, the signal selected by selecting circuit 60 and output to synchronizing pattern detecting circuit 90 in Suh et al. is a selected comparison signal. As shown in Fig. 2A of Suh et al. comparison circuits 40 and 50 are merely AND gates that output comparisons of parallel data, and the data output from these circuits, therefore, remains in parallel form in that it is merely a signal indicative of a comparison of parallel data. The outputs of these circuits, therefore, do not represent the data in serial form, i.e., the data is not converted back into serial data. Applicants respectfully submit that Suh et al.,

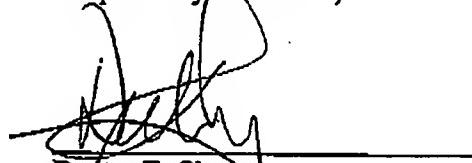
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as cited and relied upon by the Examiner, do not disclose a provisional-region detection section for sampling a part of the parallel data and outputting the provisional region data in serial form.

Applicants would like to discuss this distinction between the claimed invention and the cited reference, and any possible clarifying amendment that the Examiner may require.

Respectfully submitted,



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Docket No.: FUJS 14.330A (100794-00171)

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